RIGA TECHNICAL UNIVERSITY

Ruslans Babajans

DESIGN AND PERFORMANCE EVALUATION OF BIDIRECTIONAL ANALOG AND DISCRETE CHAOTIC OSCILLATOR SYNCHRONIZATION

Summary of the Doctoral Thesis

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RIGA TECHNICAL UNIVERSITY

Faculty of Computer Science, Information Technology and Energy

Institute of Photonics, Electronics and Telecommunications

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Doctoral Student of the Study Programme "Electronics"

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Summary of the Doctoral Thesis

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To be granted the scientific degree of Doctor of Science (Ph. D.), the present Doctoral Thesis has been submitted for the defence at the open meeting of RTU Promotion Council on 4 September 2026, at 11:00, at the Faculty of Electronics and Telecommunications of Riga Technical University, 12 Āzenes Street, Room 201.

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DECLARATION OF ACADEMIC INTEGRITY

I hereby declare that the Doctoral Thesis submitted for review to Riga Technical University for promotion to the scientific degree of Doctor of Science (Ph. D.) is my own. I confirm that this Doctoral Thesis has not been submitted to any other university for promotion to a scientific degree.

Ruslans Babajans _____

Date: _____

The Doctoral Thesis has been written in English. It consists of Introduction, five chapters, Conclusions, 72 figures, and 11 tables; the total number of pages is 103. The Bibliography contains 55 titles.

CONTENTS

ACRONYMS 6
INTRODUCTION 7
Rationale 7
The Objective Statement and the Tasks 8
Research methodology 9
Scientific Novelty and Main Results 10
The Theses to be Defended 11
The Approbation and Practical Significance 11
The Structure of the Thesis 14
1 CHAOTIC OSCILLATORS 16
1.1 Vilnius Chaotic Oscillator 16
1.2 RC Chaotic Oscillator 17
1.3 Colpitts Chaotic Oscillator 18
1.4 Simulation Models 20
1.5 Hardware Prototypes 20
2 DISCRETE CHAOTIC OSCILLATOR MODELS AND DIGITAL IMPLEMENTATION 21
2.1 Normalized Equations 21
Vilnius Chaotic Oscillator 21
RC Chaotic Oscillator 22
Colpitts Chaotic Oscillator 22
2.2 Forward Euler Numerical Integration 23
Vilnius Chaotic Oscillator 23
RC Chaotic Oscillator 23
Colpitts Chaotic Oscillator 24
2.3 Digital Design 24
2.4 Digital Design Implementation 26
3 IMPLEMENTATION AND ANALYSIS OF CHAOTIC SYNCHRONIZATION IN ANALOG-DISCRETE SYSTEMS 28
3.1 Pecora–Carroll Chaotic Synchronization 28
3.2 Study Based on Numerical Simulation 29
Analog-Discrete Synchronization 29
Discrete-Analog Synchronization 30
3.3 Study Based on hardware-in-the-loop (HiL) 30
Analog-Discrete Synchronization 31
Discrete-Analog Synchronization 31

3.4 Full Hardware Integration 32
3.5 Discussion 33
4 PERFORMANCE OF ANALOG-DISCRETE AND DISCRETE-ANALOG CHAOTIC SYNCHRONIZATION 34
4.1 Synchronization Noise Immunity 34
Analog-Discrete Synchronization 34
Discrete-Analog Synchronization 35
Study Results 35
Discrete-Discrete Synchronization Comparison 36
4.2 Synchronization and De-synchronization Time 37
Analog-Discrete and Discrete-Analog Simulation and Experimental Setup . 37
Study Results 38
4.3 Discussion 38
5 CHAOS-BASED AUTHENTICATION 39
5.1 Chaotic Oscillator Parameter Estimator-Based Hardware Authentication Scheme 39
5.2 Vilnius Chaotic Oscillator Parameter Estimator 40
Digital Implementation of the Parameter Estimator 40
Performance Evaluation 42
5.3 Discussion 44
CONCLUSIONS 45
Bibliography 46

ACRONYMS

ALM adaptive logic module

B.L.AWGN band-limited additive white Gaussian noise

BRAM block random access memory

DSP digital signal processing

FPGA field-programmable gate array

HiL hardware-in-the-loop

IoT Internet-of-Things

LMS least mean squares

LUT lookup table

MMSE minimum mean squared error

PCB printed circuit board

PLA physical-layer authentication

PSD power spectral density

ROM read-only memory

SNR signal-to-noise ratio

VHDL very high-speed integrated circuit (VHSIC) hardware description language

WSN wireless sensor network

INTRODUCTION

Rationale

The rapid evolution of the Internet-of-Things (IoT) has transformed modern technological ecosystems into highly interconnected and data-driven environments. IoT systems integrate heterogeneous devices, sensors, and communication infrastructures to enable continuous monitoring, automation, and intelligent decision-making across domains such as healthcare, smart cities, and industrial automation [1]. These systems generate and exchange vast volumes of data, often in real time, creating significant opportunities for efficiency, scalability, and innovation.

However, this rapid expansion also introduces fundamental challenges. IoT architectures are inherently resource-constrained, highly distributed, and typically operate in open and potentially hostile communication environments. As a result, they are particularly vulnerable to security threats. Ensuring data confidentiality, integrity, and authenticity is therefore a critical requirement, especially in applications involving sensitive information such as medical or industrial data [2]–[4]. Conventional cryptographic approaches, while effective, may not always be suitable for IoT scenarios due to their computational complexity, energy consumption, and scalability limitations.

In this context, chaos theory offers a promising addition to secure communication and information processing. Chaotic systems are governed by deterministic nonlinear dynamics, yet exhibit properties such as sensitivity to initial conditions, broadband spectra, and pseudo-random behavior. These characteristics make them inherently suitable for generating complex, noise-like signals that are difficult to predict or reconstruct without precise system knowledge [5]. Consequently, chaos-based techniques have gained increasing attention as lightweight and hardware-efficient solutions for security in constrained environments.

The application of chaos theory has expanded significantly across engineering domains, particularly in areas requiring secure data transmission and processing. In IoT systems, chaos has been successfully applied to:

- cryptography and data encryption, where chaotic maps and oscillators generate highly unpredictable sequences for encryption of multimedia and sensor data [6]–[8];
- secure communication systems, including chaos-based modulation schemes that improve robustness against noise and interception [9]–[11];
- random number generation, where chaotic dynamics serve as entropy sources for cryptographic primitives [12]–[14].

These applications exploit key properties of chaotic signals, such as ergodicity, unpredictability, and wideband spectrum, which closely align with the requirements of secure and efficient IoT operation. Moreover, chaos-based methods often exhibit low computational complexity and high parallelism, making them particularly suitable for hardware implementation in resource-limited environments.

From an implementation perspective, chaotic behavior can arise in a wide range of electronic systems, including analog oscillators described by nonlinear differential equations [15], discrete maps [16], switching power converters [17]–[19], phase-locked loops [20], and memristive systems [21], [22]. Each of these realizations introduces specific design trade-offs, particularly regarding the distinction between analog and digital implementations of chaos.

Analog chaotic systems, typically realized using electronic circuits, offer advantages such as large bandwidth, continuous-time operation, and low power consumption. However, they are sensitive to noise, component tolerances, and parameter drift, which can affect reproducibility and long-term stability. In contrast, discrete chaotic systems provide precise control over system parameters and initial conditions, as well as robustness to environmental variations and ease of integration with digital platforms such as microcontrollers and field-programmable gate arrays (FPGAs). Nevertheless, digital implementations are inherently limited by finite precision and quantization effects, which may degrade chaotic properties and reduce entropy if not properly addressed.

Recent studies, including [23], [24], highlight a growing trend toward hybrid approaches that combine analog chaotic signal generation with digital processing and control. Such architectures aim to leverage the high entropy and bandwidth of analog chaos while benefiting from the flexibility, scalability, and reproducibility of digital systems. For instance, analog chaotic signals can be digitized using comparators or analog-to-digital converters and subsequently processed in digital hardware for encryption, synchronization, or communication tasks.

This duality underscores the importance of studying analog and discrete chaotic systems within a unified framework, particularly in the context of synchronization. Chaotic synchronization plays a central role in many applications, including secure communication and signal reconstruction. Existing studies predominantly focus on synchronization between either purely analog systems or purely discrete models [25]–[28]. While significant progress has been made in both domains, comparatively less attention has been given to synchronization between heterogeneous systems, such as analog and discrete chaotic oscillators.

Furthermore, prior works have addressed practical implementations of chaotic systems and synchronization on FPGAs and other digital platforms [6], [29]–[34]. However, the integration of analog and discrete chaotic systems into a unified hybrid synchronization framework remains an open and relevant research problem.

The Objective Statement and the Tasks

The **objective** of this Doctoral Thesis is to develop and evaluate a framework for synchronization between heterogeneous chaotic systems, specifically analog and discrete chaotic oscillators.

The following **tasks** are stated to achieve the previously defined objective:

- to develop mathematical models and hardware-efficient digital designs for the Vilnius, RC,

and Colpitts chaotic oscillators, optimized for FPGA implementation;

- to investigate Pecora–Carroll synchronization between analog implementations and their discrete counterparts through numerical simulations, HiL setups, and full hardware integration;
- to assess the noise immunity and the time required for synchronization and de-synchronization across these hybrid systems;
- to design and implement a chaos-based authentication system utilizing a parameter estimator for the Vilnius oscillator, demonstrating the practical application of chaotic synchronization in secure communications.

Research Methodology

This research follows a combined analytical, numerical, and experimental methodology to investigate synchronization between analog and discrete chaotic oscillators. The methodological framework is structured into several sequential stages, ensuring both theoretical rigor and practical validation.

First, mathematical models of the selected chaotic oscillators (Vilnius, RC, and Colpitts) are developed. The governing nonlinear differential equations are derived using circuit laws and normalized to enable efficient numerical processing. These models serve as the foundation for both simulation and digital implementation.

Second, numerical simulation and analysis are conducted using circuit simulation tools and MATLAB-based post-processing. Analog oscillator models are implemented in LTspice, and their dynamical behavior is analyzed through time-domain signals, phase-space attractors, and power spectral density (PSD). To enable digital realization, the analog oscillator models are discretized using numerical integration methods, specifically the forward Euler method, with careful consideration of stability and accuracy.

Third, digital design and implementation of the discrete chaotic oscillators are carried out on FPGA platforms. Fixed-point arithmetic is employed to ensure resource-efficient hardware realization while preserving essential chaotic properties. Dedicated architectures, such as derivative calculation pipelines and lookup table (LUT)-based nonlinear function implementations, are developed to optimize performance.

Fourth, synchronization analysis is performed using the Pecora–Carroll drive–response framework. Several synchronization configurations are investigated, primarily analog-discrete and discrete-analog. These studies are conducted across three levels:

- pure numerical simulations;
- HiL setups;
- full hardware integration involving physical circuits and FPGA implementations.

Fifth, experimental validation is conducted using fabricated printed circuit board (PCB) proto-

types of the analog oscillators and FPGA-based digital systems. Measurement equipment is used to acquire real-time signals, which are then analyzed and compared with simulation results to verify consistency and accuracy.

Sixth, performance evaluation is carried out to assess synchronization quality under non-ideal conditions. Key metrics include:

- Pearson correlation coefficient for synchronization accuracy;
- noise immunity under additive disturbances;
- synchronization and de-synchronization time;
- sensitivity to parameter mismatch and quantization effects.

Finally, application-oriented validation is performed by developing a chaos-based authentication scheme. A parameter estimation approach based on adaptive filtering (least mean squares algorithm) is implemented and evaluated, demonstrating the feasibility of using chaotic synchronization in physical-layer authentication.

Overall, the methodology integrates theoretical modeling, simulation-based analysis, hardware design, and experimental validation into a unified framework, enabling a comprehensive investigation of hybrid analog-discrete chaotic systems.

Scientific Novelty and Main Results

The scientific novelty of this Thesis lies in integrating analog and discrete chaotic systems into a unified hybrid synchronization framework. This topic has received limited attention in prior research. The main results of the work include:

- for the first time, the experimental validation of stable synchronization between physical analog circuits and their discrete counterparts implemented on an FPGA;
- a comprehensive study of synchronization properties in hybrid configurations, demonstrating that a high correlation (above 0.8) can be maintained even in non-ideal environments;
- the development of a digital parameter estimator for the Vilnius chaotic oscillator, which is a hardware-efficient solution for physical-layer authentication.

In addition to the scientific contributions, this Thesis provides several important practical and methodological results.

- The development of ”Derivative Calculation Pipelines” and fixed-point models that preserve chaotic attractors despite the limitations of digital quantization.
- Establishing a methodology for comparing hybrid synchronization performance against purely discrete benchmarks using the Pearson correlation coefficient.

The Theses to be Defended

1. Chaotic synchronization between analog and discrete implementations of nonlinear oscillators is achievable in both analog-discrete and discrete-analog configurations under unidirectional Pecora-Carroll coupling, provided that time-domain alignment, the analog-digital interface satisfies sufficient sampling rate, quantization resolution, and bandwidth constraints to preserve the underlying system dynamics.
2. In the Vilnius and RC chaotic oscillators, hybrid synchronization converges more slowly than it diverges; moreover, state variables with stronger coupling to the synchronization signal attain higher synchronization quality and faster convergence.
3. Estimation of a drive chaotic oscillator's parameter that appears in the difference equation as a weighting coefficient is achievable by applying the adaptive least mean squares filter to the response oscillator corresponding parameter evaluated from state variables.

The Approbation and Practical Significance

The results presented in this Doctoral Thesis were obtained within the framework of applied research and experimental development activities carried out by the author during doctoral studies at Riga Technical University. The research evolved in close connection with ongoing academic, industrial, and applied research projects, ensuring both scientific relevance and practical applicability of the studied hybrid synchronization.

The scientific results of this Thesis have been published in peer-reviewed international journals and conference proceedings. The most significant publications directly reflecting the core contributions of this Thesis are listed below. Publications in which the author is the first author are highlighted in **bold**.

[35] R. Babajans et al. "Study on Analog and Discrete Chaos Oscillators Synchronization." en. In: *16th Chaotic Modeling and Simulation International Conference*. Ed. by C. H. Skiadas and Y. Dimotikalis. Cham: Springer Nature Switzerland, 2024, pp. 33–46. ISBN: 978-3-031-60907-7. DOI: 10.1007/978-3-031-60907-7_4

[36] R. Babajans et al. "Experimental Study on Analog and Discrete Chaos Oscillators Synchronization." In: *2023 Workshop on Microwave Theory and Technology in Wireless Communications (MTTW)*. Oct. 2023, pp. 24–28. DOI: 10.1109/MTTW59774.2023.10319995

[37] R. Babajans et al. "Synchronization of Analog-Discrete Chaotic Systems for Wireless Sensor Network Design." en. In: *Applied Sciences* 14.2 (Jan. 2024). Number: 2, p. 915. ISSN: 2076-3417. DOI: 10.3390/app14020915

[38] R. Babajans, D. Cirjulina, and D. Kolosovs. "Discrete Sequential Implementation of Chaos Oscillators for FPGA Integration." In: *2024 IEEE Workshop on Microwave Theory and Technology in Wireless Communications (MTTW)*. Riga, Latvia: IEEE, Oct. 2024, pp. 33–

36. ISBN: 979-8-3315-3317-5. DOI: 10.1109/MTTW64344.2024.10742168

[39] R. Babajans, D. Cirjulina, and D. Kolosovs. "Field-Programmable Gate Array-Based Chaos Oscillator Implementation for Analog–Discrete and Discrete–Analog Chaotic Synchronization Applications." en. In: *Entropy* 27.4 (Apr. 2025). Number: 4, p. 334. ISSN: 1099-4300. DOI: 10.3390/e27040334

[40] R. Babajans et al. "Noise Performance Study of FPGA-based and Analog Chaos Oscillator Synchronization." en. In: *2025 IEEE 12th Workshop on Advances in Information, Electronic and Electrical Engineering (AIEEE)*. Vilnius, Lithuania: IEEE, 2025, pp. 1–5. DOI: 10.1109/AIEEE66149.2025.11050878

[41] D. Cirjulina et al. "Nonlinear Dynamics and Hybrid Synchronization of DC Biased Colpitts Chaotic Oscillators." en. In: *Electronics* 14.20 (Jan. 2025), p. 4005. ISSN: 2079-9292. DOI: 10.3390/electronics14204005

[42] R. Babajans et al. "Chaos-Based Dynamical Parameter Estimation for Physical Layer Authentication in Wireless IoT Networks." en. In: *Electronics* 15.4 (Jan. 2026), p. 748. ISSN: 2079-9292. DOI: 10.3390/electronics15040748

The research results of this Thesis were also presented at international scientific conferences, workshops, and symposia, providing peer feedback and dissemination within the research community. The author presented the results of this Doctoral Thesis at the following international scientific conferences.

- R. Babajans "Synchronization of Analog and Discrete Chaos Oscillators," Days of Applied Nonlinearity and Complexity (DANOC 2024), Greece, Thessaloniki, 12–14 January 2024.
- R. Babajans "FPGA-based Chaos Oscillator Parameter Estimator for Data Transfer," Days of Applied Nonlinearity and Complexity (DANOC 2026), Aristotle University of Thessaloniki, Thessaloniki, Greece, 23–25 January 2026.
- R. Babajans "Discrete Sequential Implementation of Chaos Oscillators for FPGA Integration," 2024 Workshop on Microwave Theory and Technology in Wireless Communications (MTTW 2024), IEEE Latvia Section COM/MTT/AP Joint Society Chapter, IEEE Latvia Section, Riga Technical University, Riga 2–4 October 2024.
- R. Babajans "Experimental Study on Analog and Discrete Chaos Oscillators Synchronization," 2023 Workshop on Microwave Theory and Technology in Wireless Communications (MTTW 2023), IEEE Latvia Section COM/MTT/AP Joint Society Chapter, IEEE Latvia Section, Riga Technical University, Riga, 4–6 October 2023.
- R. Babajans "Quadrature Chaos Phase Shift Keying Communication System Based on Vilnius Chaos Oscillator," 2022 Workshop on Microwave Theory and Technology in Wireless Communications (MTTW 2022), IEEE Latvia Section COM/MTT/AP Joint Society Chapter, IEEE Latvia Section, Riga Technical University, Riga, 5–7 October 2022.
- R. Babajans "Noise Performance Study of FPGA-based and Analog Chaos Oscillator Syn-

chronization," 2025 IEEE 12th Workshop on Advances in Information, Electronic and Electrical Engineering (AIEEE 2025), Lithuania, Vilnius, 15–17 May 2025.

- R. Babajans "Noise Performance Study of FPGA-based and Analog Chaos Oscillator Synchronization," RTU 66th International Scientific Conference, Riga Technical University, Riga, Latvia, 27 November 2025.
- R. Babajans "FPGA-based Chaos Oscillator Implementation for Analog-Discrete and Discrete-Analog Chaotic Synchronization Applications," RTU 66th Student Scientific and Technical Conference, Riga Technical University, Riga, Latvia, 25 April 2025.
- R. Babajans "Synchronization of Analog and Discrete Chaos Oscillators," RTU 65th International Scientific Conference, Riga Technical University, Riga, Latvia, 11 October 2024.
- R. Babajans "Study on Analog and Discrete Chaos Oscillators Synchronization," The 16th CHAOS 2023 International Conference, Technical University of Crete, Crete, Greece, 13–17 June 2023.

The research was conducted in parallel with participation in several national and institutional research projects, which supported the experimental validation, prototype development, and applied investigations addressed in this Thesis.

1. "Implementation of consolidation and management changes at RTU, LiepU, Rēzekne Academy of Technology and Latvian Maritime Academy and Liepāja Maritime College for progress towards excellence in higher education, science and innovation." Grant No RTU-PA-2024/1-0064 under the EU RRF project No. 5.2.1.1.i.0/2/24/I/CFLA/003 (01.01.2024 – 31.01.2026).
2. SAM 8.2.2. "Strengthening of Ph. D. students and academic personnel of Riga Technical University and BA School of Business and Finance in the strategic fields of specialization" of the Specific Objective 8.2.2 "To Strengthen Academic Staff of Higher Education Institutions in Strategic Specialization Areas" of the Operational Program "Growth and Employment" and the RTU doctoral grant program. Project 03000-3.1.2.1-e/177 | 8.2.2.0/20/I/008. (01.12.2022–30.11.2023).
3. LZP fundamental and applied research project "Advanced wireless power transmission techniques" 03000-3.1.2.1-e/4 | lzp-2021/1-0170 (03.01.2022–30.12.2024).
4. "Exploring the Next Generation IoT Network", 03000-3.1.2.1-e/14 edoc | ZI-2023/3 | 4691, Internal funding of RTU (02.01.2023 – 31.12.2023).
5. "Exploring cyber-secure IoT data-driven agricultural management", 04000-1.3-e/24 | ZI-2024/7 | 4834, Internal funding of RTU (02.01.2024 – 31.12.2024).
6. "RTU Doctoral Grants for Supporting Scientific Excellence in Smart Specialization Areas" 0B000-3.5.3-e/3 | 1.1.1.8/1/24/I/007 | 5021, within the framework of a doctoral grant ID 8024 (15.09.2025 – 15.09.2026).

During the Doctoral studies, the author has been involved in teaching the following study courses at Riga Technical University.

- REA711 – Fundamentals of Digital Electronic Systems Design using HDL (4.5 ECTS).
- DE0092 – Simulation of Functional and Logical Circuits (4 ECTS).
- DE0735 – Signal Processing Systems (Study work) (3 ECTS).
- REA712 – Fundamentals of Digital Electronic Systems Design using HDL (study project) (3 ECTS).
- RTR822 – Signal Theory (4.5 ECTS).
- DE0101 – Signal Processing Systems (4 ECTS).
- DE0103 – Electronic Systems for Data Transmission (4 ECTS).
- DE0501 – Signal Theory (study project) (3 ECTS).

The development of this Doctoral Thesis was further supported by international academic and research mobility, enabling collaboration with external research institutions and access to advanced experimental infrastructure. During the doctoral studies, the author remained employed at Riga Technical University while completing the following mobility periods:

- KTH Royal Institute of Technology, Sweden (01.05.2023–31.05.2023);
- Politecnico di Torino, Italy (18.11.2024–22.11.2024);
- Aristotle University of Thessaloniki, Greece (30.11.2025–05.12.2025).

The scientific and academic contributions of the author during doctoral studies was recognized by the following award:

- Best Paper Award, 2023 Workshop on Microwave Theory and Technology in Wireless Communications, 06.10.2023.

Overall, the results presented in this Doctoral Thesis were validated through peer-reviewed publications, international conference presentations, experimental prototypes, and applied research projects. The combination of simulation-based analysis and experimental measurements confirms the scientific relevance and practical applicability of the hybrid analog-discrete, discrete-analog synchronization.

The Structure of the Thesis

The first chapter provides an overview of chaotic oscillators, including the Vilnius, RC, and Colpitts chaotic oscillators. Mathematical models are developed, and their dynamical properties are analyzed through numerical simulations and experimental validation.

The second chapter focuses on discrete-time modeling of chaotic oscillators and their implementation in digital hardware. Particular attention is given to FPGA-based realization, fixed-point arithmetic, and the preservation of chaotic behavior in digital form.

The third chapter investigates synchronization between analog and digital chaotic systems. Various configurations are examined, including analog-discrete, discrete-analog, with results obtained from simulations and experimental platforms.

The fourth chapter presents a comprehensive performance analysis of the proposed systems. Key aspects such as synchronization accuracy, robustness to noise, parameter mismatch, and transient behavior are evaluated.

The fifth chapter explores the application of chaotic systems in physical-layer authentication. A stochastic gradient-based parameter estimation technique is used to demonstrate the feasibility of chaos-based physical-layer security mechanisms.

Together, these sections establish a unified framework for the analysis and implementation of chaotic systems, bridging analog and digital domains and highlighting their applicability in synchronization and physical-layer security.

1 CHAOTIC OSCILLATORS

This chapter explores three analog chaotic oscillators: the Vilnius [43], RC [44] and Colpitts [45]. Each oscillator is analyzed through its circuit structure, LTspice simulation models, and experimental hardware prototypes. The comparison between simulated and measured results provides a foundation for the practical realization of chaotic dynamics, which are characterized by deterministic equations, sensitivity to initial conditions, and noise-like spectral properties.

To achieve chaos in analog electronics, a system must possess at least three reactive elements and a nonlinear element. The specific oscillators selected for this Thesis were chosen for their compatibility with low-voltage (≤ 5 V) embedded applications, minimal component count, and the ability to scale dynamics to higher frequencies for data transmission. By featuring distinct design architectures, this selection demonstrates that the methodologies developed in this Thesis are applicable across diverse chaotic systems.

1.1 Vilnius Chaotic Oscillator

The first oscillator selected for this Thesis is the Vilnius chaotic oscillator [43]. Its primary advantage lies in its relatively simple circuit structure, which features a clear separation between the linear resonant network and the nonlinear element. The LC resonant network ensures stable oscillatory dynamics and well-defined frequency characteristics, simplifying both tuning and analysis. Furthermore, the circuit operates efficiently at low supply voltages and requires minimal active components, resulting in low power consumption and reliable hardware implementation.

The circuit diagram of the Vilnius chaotic oscillator is presented in Fig. 1.1. The oscillator contains the fundamental building blocks required for chaotic behavior in electronic systems.

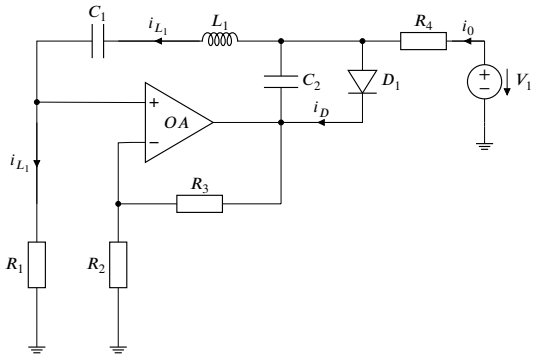


Fig. 1.1. Vilnius chaotic oscillator circuit diagram.

The oscillator dynamics is described by three state variables: the voltage across the capacitor C_1 (v_{C_1}), the current through the inductor L_1 (i_{L_1}), and the voltage across the capacitor C_2 (v_{C_2}). The set of nonlinear differential equations derived from Kirchhoff's laws of the oscillator is:

$$\begin{cases} C_1 \dfrac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = i_{L_1} \\ L_1 \dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = (k-1) \cdot R_1 \cdot i_{L_1} - v_{C_1} - v_{C_2} \\ C_2 \dfrac{\mathrm{d}v_{C_2}}{\mathrm{d}t} = i_0 + i_{L_1} - i_D \end{cases}, \tag{1.1}$$

where i_D is the current through diode D_1; i_0 is the current through resistor R_4; and k is the gain of the non-inverting operational amplifier circuit. The nonlinear behavior arises from the current-voltage characteristic of the diode, expressed as

$$i_D = i_S \cdot \left(\mathrm{e}^{\frac{v_{C_2}}{V_T}} - 1 \right), \tag{1.2}$$

where i_S is the diode saturation current (approximately 2×10^{-14} A for a 1N4148 diode), and V_T is the thermal voltage (approximately 26 mV at room temperature of 298 K).

The chaotic oscillator has the following parameter values: $C_1 = 1$ nF, $C_2 = 150$ pF, $L_1 = 1$ mH, $R_1 = 1$ kΩ, $R_2 = 10$ kΩ, $R_3 = 6$ kΩ, $R_4 = 20$ kΩ, $V_1 = 5$ V and $k = 1.6$.

1.2 RC Chaotic Oscillator

The second chaotic oscillator selected is the RC chaotic oscillator [44]. A primary advantage of this design is its reliance on resistors, capacitors, operational amplifiers, and a diode, allowing for a compact and cost-effective implementation. By excluding inductors, the circuit significantly reduces overall size and eliminates challenges such as magnetic coupling and component variability. These characteristics, combined with its reliable performance at low supply voltages, make the RC oscillator highly suitable for low-power analog systems and integrated circuit implementations.

The circuit diagram of the RC chaotic oscillator is presented in Fig. 1.2. The oscillator is based on a Wien bridge configuration and incorporates the essential components required for chaotic dynamics in electronic systems.

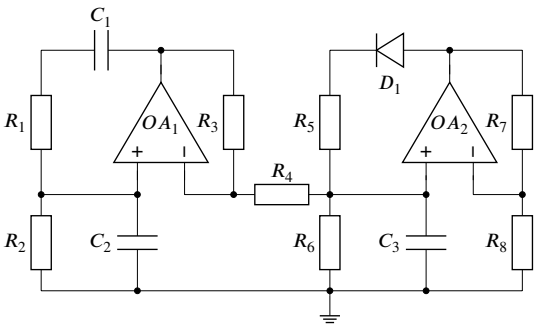


Fig. 1.2. RC chaotic oscillator circuit diagram.

The mathematical model of the RC chaotic oscillator is derived from Kirchhoff's current law applied to each capacitor node:

$$\begin{cases} C\frac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = -\frac{v_{C_1}}{R} + \frac{k_1-1}{R}v_{C_2} - \frac{k_1-1}{R}v_{C_3} \\ C\frac{\mathrm{d}v_{C_2}}{\mathrm{d}t} = -\frac{v_{C_1}}{R} + \frac{k_1-2}{R}v_{C_2} - \frac{k_1-1}{R}v_{C_3} \\ C\frac{\mathrm{d}v_{C_3}}{\mathrm{d}t} = \frac{k_1}{R}v_{C_2} - \frac{k_1+\alpha}{R}v_{C_3} + \frac{\beta}{R}(v_{C_3} - v^*)H(v_{C_3} - v^*) \end{cases}, \tag{1.3}$$

where the introduced parameters are defined as follows:

$$\begin{aligned} &k_1 = \frac{R_3}{R_4} + 1, \qquad k_2 = \frac{R_7}{R_8} + 1, \qquad \alpha = \frac{R_1}{R_6}, \qquad \beta = \frac{R_1}{R_8}, \\ &v^* = \frac{v_0}{k_2-1}, \quad C_1 = C_2 = C_3 = C, \quad R_1 = R_2 = \left(R_3 + R_4\right) = R. \end{aligned} \tag{1.4}$$

The nonlinearity of the oscillator is introduced by a diode in the feedback loop. The characteristic voltage v^* is defined by the diode's forward voltage drop v_0 (typically 0.7 V), and the nonlinear behavior is analytically modeled using the Heaviside step function:

$$H = \begin{cases} 0, & \text{if } v_{C_3} - v^* < 0 \\ 1, & \text{if } v_{C_3} - v^* \geq 0 \end{cases}. \tag{1.5}$$

For the RC chaotic oscillator, the fundamental frequency is determined by the Wien bridge network composed of R_1,R_2,C_1, and C_2. The original study [44] introduced the circuit with the following parameters: $C_1 = C_2 = C_3 = 1.3$ nF, $R_1 = R_2 = 11$ kΩ, $R_3 = 9.1$ kΩ, $R_4 = 2$ kΩ, $R_5 = R_7 = 2.7$ kΩ, $R_6 = 1.1$ kΩ, $R_8 = 780$ Ω, the diode is 1N4148.

1.3 Colpitts Chaotic Oscillator

The third oscillator used in this Thesis is the Colpitts chaotic oscillator [45]. A key advantage of this oscillator is its high-frequency capability and efficient energy transfer within the LC tank circuit. Compared with op-amp-based chaotic oscillators, transistor-based Colpitts oscillator can achieve higher operating frequencies and improved energy efficiency. The circuit also requires a relatively small number of components and can operate from low supply voltages, making it suitable for compact hardware implementations and potential RF or communication-related applications.

The circuit diagram of the Colpitts chaotic oscillator is shown in Fig. 1.3. The circuit incorporates the essential components required for the generation of chaotic dynamics in an analog circuit.

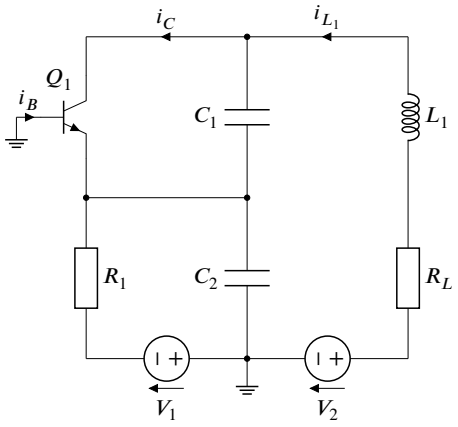


Fig. 1.3. Colpitts chaotic oscillator circuit diagram.

Applying Kirchhoff's laws to the circuit yields the following nonlinear differential equations:

$$\begin{cases} C_1 \dfrac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = i_{L_1} - i_C \\ C_2 \dfrac{\mathrm{d}v_{C_2}}{\mathrm{d}t} = \dfrac{V_1 - v_{C_2}}{R_1} - i_{L_1} - i_B \\ L_1 \dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = V_2 - v_{C_1} - v_{C_2} - i_{L_1} \cdot R_L \end{cases} . \tag{1.6}$$

In these equations, i_B and i_C are nonlinear functions describing the transistor's operation. The transistor Q_1 alternates between the forward-active region and cutoff. A piecewise-linear approximation for the transistor currents is given by:

$$i_B = \begin{cases} 0, & \text{if } -v_{C_2} \le V_{TH} \\ -\dfrac{v_{C_2} + V_{TH}}{R_{ON}}, & \text{if } -v_{C_2} > V_{TH} \end{cases} , \tag{1.7}$$

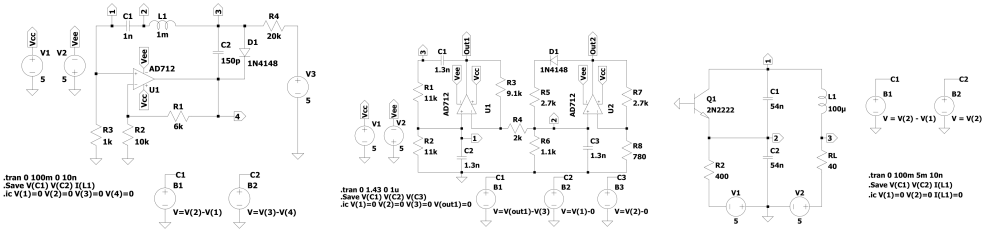
$$i_C = \beta_F \cdot i_B, \tag{1.8}$$

where V_{TH} is the base-emitter threshold voltage, R_{ON} is the small-signal on-resistance of the base-emitter junction, and β_F is the transistor's forward current gain.

The circuit parameters are as follows: $V_1 = 5\,\mathrm{V}$, $V_2 = 5\,\mathrm{V}$, $R_L = 40\,\Omega$, $L_1 = 100\,\mu\mathrm{H}$, $C_1 = 54\,\mathrm{nF}$, $C_2 = 54\,\mathrm{nF}$, and $R_1 = 400\,\Omega$, the transistor is 2N2222.

1.4 Simulation Models

To evaluate the behavior of the selected chaotic oscillators, LTspice models were developed for the Vilnius, RC, and Colpitts architectures, as illustrated in Fig. 1.4. The simulation durations and maximum time steps were tailored to each oscillator: the Vilnius and Colpitts models were configured for 100 ms with a 10 ns step, while the RC oscillator was set to 1.43 s with a 1 μs step. Due to the adaptive time-stepping algorithm utilized by the LTspice solver, the raw simulation data features non-uniform intervals. To ensure compatibility for further processing, the exported signals were resampled in MATLAB to generate a uniformly spaced time series.

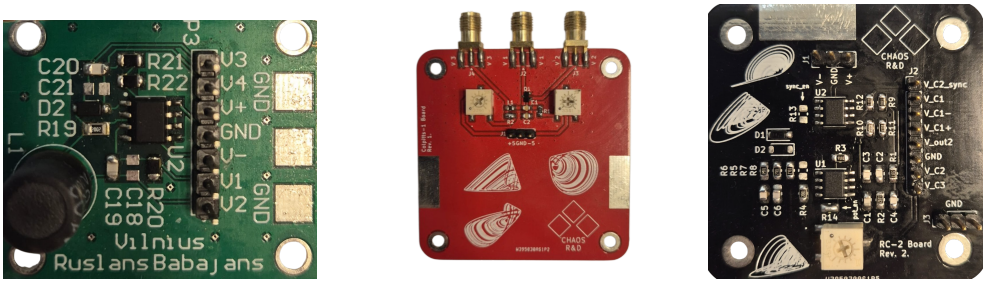


(a) (b) (c)

Fig. 1.4. LTspice models of the Vilnius (a), RC (b) and Colpitts (c) chaotic oscillators.

1.5 Hardware Prototypes

For this Thesis, hardware prototypes of the Vilnius, RC, and Colpitts oscillators were developed. Each PCB was designed using KiCad and fabricated on two-layer FR4 substrates, as shown in Fig. 1.5. Across all three oscillators, the hardware implementations demonstrated strong qualitative agreement with their LTspice counterparts. In this Thesis, the LTspice models serve as the primary tool for initial behavioral modeling and parameter optimization, while the physical prototypes are used for final hardware verification.



(a) (b) (c)

Fig. 1.5. Fabricated hardware prototypes of the Vilnius (a), RC (b) and Colpitts (c) chaotic oscillators.

2 DISCRETE CHAOTIC OSCILLATOR MODELS AND DIGITAL IMPLEMENTATION

This chapter presents the transformation of analog chaotic oscillator models into discrete-time representations and their implementation on FPGA platform. Continuous-time dynamics, described by nonlinear differential equations, are approximated using numerical integration method to obtain discrete models suitable for digital implementation.

Digital implementations enable precise control of parameters and initial conditions and are robust to environmental variations, though they are limited by finite precision, quantization, and sampling effects. A key step in the process is the normalization of equations, which reduces dynamic range and supports efficient fixed-point implementation.

Overall, this framework enables consistent modeling, comparison, and hardware realization of chaotic oscillators for applications such as secure communication.

2.1 Normalized Equations

The first step in FPGA implementation of chaotic oscillator models is the normalization of differential equations. This process converts variables and parameters into dimensionless forms with bounded ranges and introduces normalized time based on a characteristic system constant. As a result, the equations become simpler and independent of physical units, making them suitable for digital realization. Normalization ensures compatibility with finite word-length constraints, improves numerical stability, and reduces the risk of overflow. It also enables efficient use of hardware resources and allows flexible control of system dynamics through the choice of the integration step size.

Vilnius Chaotic Oscillator

In the case of Vilnius chaotic oscillator, the following parameters are introduced to acquire the normalized (dimensionless) form of the equations:

$$\begin{gathered} x = \frac{v_{C_1}}{V_T}, \quad y = \frac{\rho \cdot i_{L_1}}{V_T}, \quad z = \frac{v_{C_2}}{V_T}, \quad V_T = \frac{k_B T}{e}, \quad \rho = \sqrt{\frac{L_1}{C_1}}, \quad \varepsilon = \frac{C_2}{C_1}, \\ a = (k-1)\frac{R_1}{\rho}, \quad b = \frac{\rho \cdot i_0}{V_T}, \quad c = \frac{\rho \cdot i_S}{V_T}, \quad \theta = \frac{t}{\tau}, \quad \tau = \sqrt{L_1 \cdot C_1}. \end{gathered} \tag{2.1}$$

Using these substitutions, the system can be expressed in normalized form:

$$\begin{cases} \frac{\mathrm{d}x}{\mathrm{d}\theta} = y \\ \frac{\mathrm{d}y}{\mathrm{d}\theta} = a \cdot y - x - z \\ \varepsilon \cdot \frac{\mathrm{d}z}{\mathrm{d}\theta} = b + y - c \cdot (\mathrm{e}^z - 1) \end{cases} . \tag{2.2}$$

The resulting system is fully expressed in dimensionless variables and time, making it independent of physical units. This normalized representation is well suited for digital implementation, as it ensures bounded signal ranges and enables further realization of the Vilnius chaotic oscillator on an FPGA.

RC Chaotic Oscillator

In the case of the RC chaotic oscillator, the original set of nonlinear differential equations is transformed using the following parameters:

$$x = \frac{v_{C_1}}{v^*}, \quad y = \frac{v_{C_2}}{v^*}, \quad z = \frac{v_{C_3}}{v^*}, \quad \theta = \frac{t}{\tau}, \quad \tau = R \cdot C. \tag{2.3}$$

Using these substitutions, the system can be rewritten in normalized form:

$$\begin{cases} \frac{\mathrm{d}x}{\mathrm{d}\theta} = -x + \left(k_1 - 1\right) \cdot y - \left(k_1 - 1\right) \cdot z \\ \frac{\mathrm{d}y}{\mathrm{d}\theta} = -x + \left(k_1 - 2\right) \cdot y - \left(k_1 - 1\right) \cdot z \\ \frac{\mathrm{d}z}{\mathrm{d}\theta} = k_1 \cdot y - \left(k_1 + \alpha\right) \cdot z + \beta \cdot (z - 1) \cdot H\left(z - 1\right) \end{cases}. \tag{2.4}$$

With the applied transformation, the resulting system is expressed in dimensionless variables and time. Like in the case of the Vilnius chaotic oscillator, the differential equations of the RC chaotic oscillator in normalized representation are well-suited for further digital implementation.

Colpitts Chaotic Oscillator

The differential equations of the Colpitts chaotic oscillator are transformed using the following variables, which were derived specifically for this Thesis:

$$\begin{aligned} & i_{L_1} \cdot \rho_1 = \tilde{i}_{L_1}, \quad i_B \cdot \rho_1 = \tilde{i}_B, \qquad \frac{\omega_1}{\rho_1} = \frac{1}{L_1}, \qquad \epsilon = \frac{C_2}{C_1}, \\ & \frac{R_1}{\rho_1} = \tilde{R}_1, \qquad x = v_{C_1}, \qquad y = v_{C_2}, \qquad z = \tilde{i}_{L_1}, \\ & \frac{R_L}{\rho_1} = \tilde{R}_L, \qquad \rho_1 = \sqrt{\frac{L_1}{C_1}}, \quad \omega_1 = \frac{1}{\sqrt{L_1 \cdot C_1}}, \quad \tau_1 = \omega_1 \cdot t \end{aligned} \tag{2.5}$$

The simplified normalized equations of the Colpitts chaotic oscillator are:

$$\begin{cases} \frac{\mathrm{d}x}{\mathrm{d}\tau_1} = z - \beta \cdot \tilde{i}_B \\ \frac{\mathrm{d}y}{\mathrm{d}\tau_1} = -\frac{V_1 + y}{\tilde{R}_1 \cdot \epsilon} + \frac{z + \tilde{i}_B}{\epsilon} \\ \frac{\mathrm{d}z}{\mathrm{d}\tau_1} = V_2 - x - y - z \cdot \tilde{R}_L \end{cases}. \tag{2.6}$$

The acquired system (2.6) expressed in dimensionless time is further used for digital implementation.

2.2 Forward Euler Numerical Integration

Since the differential equations describe a continuous-time oscillators and the task is to design discrete-time counterparts of the oscillators, the next step is to transform the differential equations to obtain the discrete solutions of the systems. In this step, the forward Euler numerical integration is applied to acquire the approximate discrete solution for the integration step $\Delta\theta$.

Vilnius Chaotic Oscillator

In the case of Vilnius chaotic oscillator, applying the Forward Euler numerical integration yields the following difference equations:

$$\begin{cases} x[n+1] = y[n] \cdot \Delta\theta + x[n] \\ y[n+1] = (a \cdot y[n] - x[n] - z[n]) \cdot \Delta\theta + y[n] \\ z[n+1] = (b + y[n] - c \cdot (\mathrm{e}^{z[n]} - 1)) \cdot \frac{\Delta\theta}{\varepsilon} + z[n] \end{cases}, \tag{2.7}$$

where $a = 0.5$; $b = 5.769$; $c = 9.155 \cdot 10^{-5}$; $\varepsilon = 0.15$; $\Delta\theta = 2^{-10}$.

RC Chaotic Oscillator

Similarly, the discrete equations (2.8) for the RC chaotic oscillator are derived by applying forward Euler numerical integration to (2.4):

$$\begin{cases} x[n+1] = \big(\big(k_1 - 1\big) \cdot y[n] - \big(k_1 - 1\big) \cdot z[n] - x[n]\big) \cdot \Delta\theta + x[n] \\ y[n+1] = \big(\big(k_1 - 2\big) \cdot y[n] - \big(k_1 - 1\big) \cdot z[n] - x[n]\big) \cdot \Delta\theta + y[n] \\ z[n+1] = \big(k_1 \cdot y[n] - \big(k_1 + \alpha\big) \cdot z[n] + \beta \cdot (z[n] - 1) \cdot H\,(z[n] - 1)\big) \cdot \Delta\theta + z[n] \end{cases}. \tag{2.8}$$

The Heaviside step function in this case is

$$H = \begin{cases} 0, & \text{if } z[n] - 1 < 0 \\ 1, & \text{if } z[n] - 1 \geq 0 \end{cases}. \tag{2.9}$$

The final equation has the following parameters: $k_1 = 5.5$; $\alpha = 10$; $\beta = 14.1026$; $\Delta\theta = 2^{-10}$.

Colpitts Chaotic Oscillator

In the case of Colpitts chaotic oscillator, applying forward Euler numeric integration results in the following system:

$$\begin{cases} x[n+1] = \left(z[n] - \beta \cdot \tilde{i}_B\right) \cdot \Delta\theta + x[n] \\ y[n+1] = \left(-\dfrac{y[n] + V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z[n] + \tilde{i}_B}{\epsilon}\right) \cdot \Delta\theta + y[n] \\ z[n+1] = \left(V_2 - x[n] - y[n] - z[n] \cdot \tilde{R}_L\right) \cdot \Delta\theta + z[n] \end{cases} . \tag{2.10}$$

The nonlinearity in this case is

$$\tilde{i}_B = \begin{cases} 0, & \text{if } -y[n] \leq V_{TH} \\ -\dfrac{y[n] + V_{TH}}{R_{ON}} \cdot \rho_1, & \text{if } -y[n] > V_{TH} \end{cases} . \tag{2.11}$$

The final equation has the following parameters: $\beta = 200$; $\epsilon = 1$; $\rho_1 = 43.033\ \Omega$; $\tilde{R}_L = 0.9295$; $\tilde{R}_1 = 9.295$; $R_{ON} = 100\ \Omega$; $V_1 = V_2 = 5$ V; $V_{TH} = 0.75$ V; $\Delta\theta = 2^{-10}$.

2.3 Digital Design

This section describes the implementation of the chaotic oscillators' difference equations in a digital design that is intended for an FPGA. The task is to create a unified design approach that is applicable to all three chaotic oscillators. The digital design is created by outlining the mathematical operations of the difference Equations (2.7), (2.8) and (2.10) from the perspective of sequential digital design. In all three chaotic oscillator difference equations acquired via forward Euler numerical integration, the resulting system shows that the next value of the state variable is acquired from the current value of the state variable plus the derivative multiplied by the time step.

Difference equation of the Vilnius chaotic oscillator with highlighted operations:

$$\begin{cases} \underbrace{x[n+1]}_{\text{Next value}} = \underbrace{x[n]}_{\text{Current value}} + \underbrace{y[n]}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y[n+1]}_{\text{Next value}} = \underbrace{y[n]}_{\text{Current value}} + \underbrace{(a \cdot y[n] - x[n] - z[n]) \cdot}_{\text{Derivative}} \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z[n+1]}_{\text{Next value}} = \underbrace{z[n]}_{\text{Current value}} + \underbrace{\left(\frac{b}{\epsilon} + \frac{1}{\epsilon} \cdot y[n] - \frac{c}{\epsilon} \cdot (e^{z[n]} - 1)\right) \cdot}_{\text{Derivative}} \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{2.12}$$

Difference equation of the RC chaotic oscillator with highlighted operations:

$$\begin{cases} \underbrace{x[n+1]}_{\text{Next value}} = \underbrace{x[n]}_{\text{Current value}} + \underbrace{\left(\left(k_1-1\right)\cdot y[n] - \left(k_1-1\right)\cdot z[n] - x[n]\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y[n+1]}_{\text{Next value}} = \underbrace{y[n]}_{\text{Current value}} + \underbrace{\left(\left(k_1-2\right)\cdot y[n] - \left(k_1-1\right)\cdot z[n] - x[n]\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z[n+1]}_{\text{Next value}} = \underbrace{z[n]}_{\text{Current value}} + \underbrace{\left(k_1\cdot y[n] - \left(k_1+\alpha\right)\cdot z[n] + \beta\cdot(z[n]-1)\cdot H\left(z[n]-1\right)\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{2.13}$$

Difference equation of the Colpitts chaotic oscillator with highlighted operations:

$$\begin{cases} \underbrace{x[n+1]}_{\text{Next value}} = \underbrace{x[n]}_{\text{Current value}} + \underbrace{\left(z[n] - \beta\cdot\tilde{i}_B\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y[n+1]}_{\text{Next value}} = \underbrace{y[n]}_{\text{Current value}} + \underbrace{\left(-\frac{y[n]+V_1}{\tilde{R}_1\cdot\epsilon} + \frac{z[n]+\tilde{i}_B}{\epsilon}\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z[n+1]}_{\text{Next value}} = \underbrace{z[n]}_{\text{Current value}} + \underbrace{\left(V_2 - x[n] - y[n] - z[n]\cdot\tilde{R}_L\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{2.14}$$

The difference equations are mapped onto a digital circuit as shown in Fig. 2.1. The architecture utilizes registers to store and update state variables $x[n]$, $y[n]$, and $z[n]$ on every rising edge of the clock signal clk. These current states and system constants are processed by a "Derivative calculation pipeline", which computes the derivative terms with matched latency. Each derivative is multiplied by the discrete time step $\Delta\theta$, and the resulting increments are added to the current state variables to produce the next-iteration values $x[n+1]$, $y[n+1]$, and $z[n+1]$. With the presented design, the implementation difference of each chaotic oscillator is the design of the derivatives calculation pipeline.

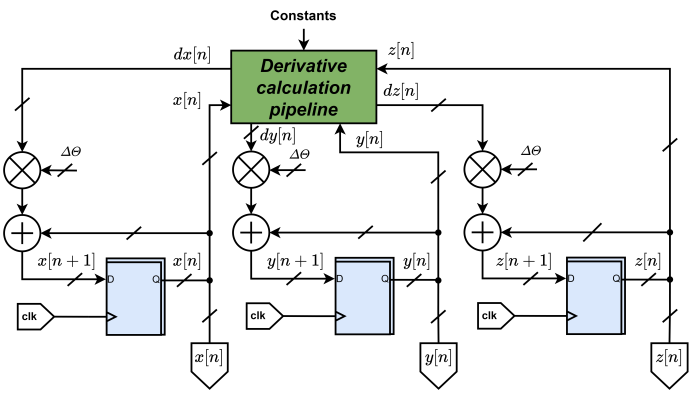


Fig. 2.1. Full digital design of chaotic oscillator system equations.

The system was initially prototyped in MATLAB to facilitate rapid debugging and verification using fixed-point arithmetic. This environment allowed for the flexible optimization of integer and fractional bit widths, which are critical for FPGA realization. The read-only memory (ROM)-based implementation of the nonlinear functions was validated in MATLAB, enabling the direct reuse of memory contents in the hardware design. The final hardware configuration utilizes a 22-bit word length, consisting of 8 integer bits and 14 fractional bits. This balance provides the dynamic range and precision necessary to preserve chaotic behavior.

2.4 Digital Design Implementation

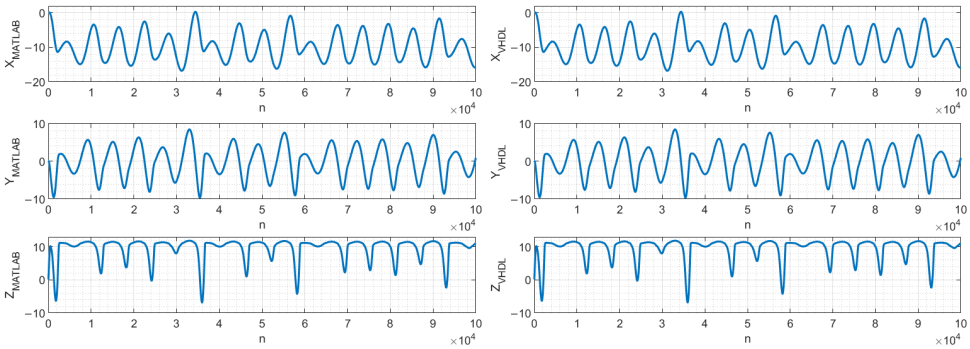
After validating the digital design in MATLAB, the system was translated into very high-speed integrated circuit (VHSIC) hardware description language (VHDL) for FPGA implementation, and consistency between both models was verified. The design targets the Altera Cyclone V 5CSXFC6D6F31C6 device, and resource utilization in terms of adaptive logic modules (ALMs), digital signal processing (DSP), and block random access memory (BRAM) is summarized in Table 2.1.

The results show that the proposed oscillators use only a small fraction of available FPGA resources, making them suitable for lower-capacity devices or integration into more complex systems. Among the designs, the RC oscillator requires slightly more ALMs and DSP blocks due to a longer pipeline, while the Colpitts oscillator has higher BRAM usage because of multiple ROMs.

Table 2.1
FPGA resource utilization of chaotic oscillators

Chaotic oscillator	**ALMs**	**DSP blocks**	**BRAM bits**
Vilnius	67 (< 1 %)	1 (1 %)	90122 (2 %)
RC	115 (< 1 %)	5 (6 %)	90122 (2 %)
Colpitts	95 (< 1 %)	1 (1 %)	180224 (3 %)

To verify that the VHDL-based design accurately reproduces the behavior of the MATLAB model, a functional simulation was performed using the Questa (ModelSim) simulation tool. The simulation results were subsequently exported to MATLAB for direct comparison. Fig. 2.2 demonstrates that, for identical parameters and initial conditions, the signals generated by the MATLAB model and the VHDL-based implementation are identical and do not diverge over 10^5 clock cycles. This indicates that the MATLAB model precisely captures the behavior of the corresponding digital design.



(a) (b)

Fig. 2.2. MATLAB (a) and VHDL-based digital design (b) Vilnius chaotic oscillator state variable signals.

The next step is the implementation of the digital designs in the hardware – the 5CSXFC6D6F31C6 FPGA chip on the DE10-Standard development board. It is important to note that in this FPGA implementation, the master clock frequency and the numerical integration step $\Delta\theta$ are not identical quantities. The FPGA system clock f_{clk} determines the rate at which arithmetic operations are executed, while $\Delta\theta$ is implemented as a constant multiplier in the discretized equations to control the effective integration step size.

The developed discrete chaotic oscillators, together with their analog counterparts, are used in subsequent studies. The chosen discretization approach, based on the forward Euler method, is sufficient to preserve the qualitative dynamics of the original analog oscillator, including the characteristic structure of chaotic attractors. Furthermore, the consistency between MATLAB and VHDL-based implementations demonstrates that the fixed-point representation and hardware realization do not introduce significant numerical distortion or instability.

Consequently, the developed discrete models accurately reproduce the behavior of their analog counterparts and can be reliably used in further investigations, including synchronization studies between analog and discrete chaotic oscillators.

3 IMPLEMENTATION AND ANALYSIS OF CHAOTIC SYNCHRONIZATION IN ANALOG-DISCRETE SYSTEMS

Chaotic synchronization, despite sensitivity to initial conditions, has important applications in secure communications and related fields. Modern systems increasingly require hybrid synchronization between continuous-time analog oscillators and discrete models or hardware implementations.

This chapter investigates bidirectional synchronization between analog and discrete chaotic systems using the Pecora–Carroll method across three stages: numerical simulation, hardware-in-the-loop, and full hardware implementation on FPGA. Synchronization performance is evaluated using Pearson correlation, demonstrating that robust synchronization can be achieved despite quantization effects and hardware non-idealities.

3.1 Pecora–Carroll Chaotic Synchronization

The first method for synchronizing chaotic systems was proposed in 1990 by Louis M. Pecora and Thomas L. Carroll in their study [46]. This synchronization technique was also called "Pecora–Carroll" synchronization. The principle of synchronization is outlined in Fig. 3.1 and is as follows: the drive system generates a chaotic signal y_1, which is then used to replace or "drive" the corresponding variable y_2 in the response system. As a result, the state variable x_2 repeats x_1, and z_2 repeats z_1. Synchronization occurs even if the initial conditions of the two chaotic systems differ.

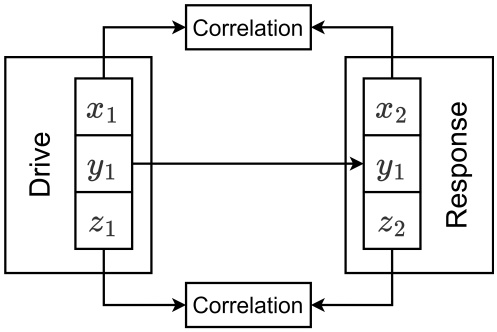


Fig. 3.1. Pecora–Carroll chaotic synchronization.

To evaluate synchronization quality, the Pearson correlation coefficient is used. This metric quantifies the similarity of the drive and response oscillator's signals. For arbitrary a and b input signals, the coefficient, denoted as r, is calculated using the following equation:

$$r = \frac{\sum_{i=1}^{n}(a_i - \bar{a})(b_i - \bar{b})}{\sqrt{\sum_{i=1}^{n}(a_i - \bar{a})^2}\sqrt{\sum_{i=1}^{n}(b_i - \bar{b})^2}}, \tag{3.1}$$

where n is the number of samples, a_i and b_i are individual samples at index i, and $\bar{a}$ and $\bar{b}$ sample means over n points.

The Pearson correlation coefficient r ranges from -1 to 1. A value of $r = 1$ indicates a perfect positive linear relationship, which remains invariant to signal scaling or shifting. Conversely, $r = -1$ signifies a perfect negative linear relationship, while $r = 0$ indicates a complete absence of linear correlation between the analyzed signals.

3.2 Study Based on Numerical Simulation

This section examines Pecora–Carroll synchronization between analog and discrete chaotic oscillators in two configurations: analog-discrete and discrete-analog. The study focuses on numerical simulations combining LTspice models of the analog oscillators and MATLAB implementations of the discrete oscillators.

To ensure compatibility, appropriate transformations are applied between dimensionless and physical domains, including scaling of amplitudes and time. This step establishes a foundation for analyzing hybrid synchronization between analog and discrete systems.

Analog-Discrete Synchronization

Fig. 3.2 demonstrates the analog-discrete synchronization configuration. The y_1 state variable of the LTspice-based drive oscillator substitutes y_2 of the MATLAB-based response discrete oscillator. As a result, x_2 should repeat the behavior of x_1, and z_2 should repeat the behavior of z_1. The synchronization's quality was evaluated using the aforementioned Pearson correlation coefficient.

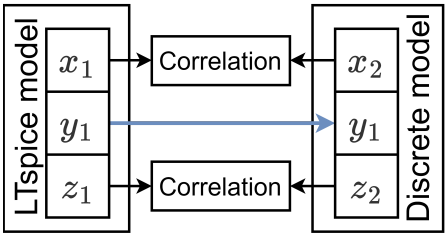


Fig. 3.2. Analog-discrete Pecora–Carroll synchronization using the LTspice and discrete models.

In the case of Vilnius and RC chaotic oscillators, this exact configuration was used – synchronization was achieved using the y state variable. In the case of Colpitts chaotic oscillators, the synchronization was done using the x state variables as synchronization signals, and synchronization was evaluated using the y and z state variables.

The Pearson correlation coefficient is computed for the 10^6 samples of synchronized signals and is presented in Table 3.1. The results compiled in Table 3.1 confirm that the analog-discrete chaotic synchronization was achieved, indicated by the Pearson correlation coefficient values exceeding 0.9.

Table 3.1
Analog-discrete synchronization evaluation using Pearson correlation coefficient

Chaotic oscillator	x_1 **and** x_2	y_1 **and** y_2	z_1 **and** z_2
Vilnius	0.99	—	0.97
RC	0.99	—	0.99
Colpitts	—	0.99	0.99

Discrete-Analog Synchronization

Fig. 3.3 demonstrates the discrete-analog synchronization configuration. The same Pecora-Carroll synchronization technique is used, but the synchronization direction is reversed compared to the previous configuration. The y_2 state variable of the MATLAB-based drive oscillator substitutes y_1 of the LTspice-based response oscillator. As a result, x_1 should repeat the behavior of x_2, and z_1 should repeat the behavior of z_2. The synchronization's quality was evaluated using the Pearson correlation coefficient.

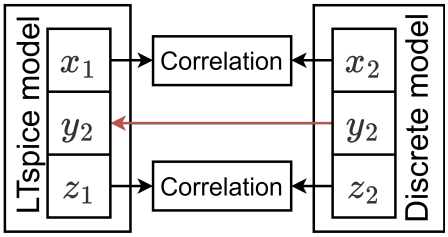


Fig. 3.3. Discrete-analog Pecora–Carroll synchronization using the LTspice and discrete models.

The Pearson correlation coefficient is computed for the 10^6 samples of synchronized signals. Table 3.2 compiles the results for the three chaotic oscillators. Table 3.2 confirms that the discrete-analog chaotic synchronization was achieved for all three chaotic oscillators, indicated by the Pearson correlation coefficient values exceeding 0.9.

Table 3.2
Discrete-analog synchronization evaluation using Pearson correlation coefficient

Chaotic oscillator	x_1 **and** x_2	y_1 **and** y_2	z_1 **and** z_2
Vilnius	0.99	—	0.97
RC	0.99	—	0.99
Colpitts	—	0.99	0.99

3.3 Study Based on HiL

The next step replaces numerical models with physical PCB-based oscillators, forming a HiL framework by interfacing hardware with MATLAB models. Both analog-discrete and discrete-analog synchronization configurations are evaluated.

To ensure compatibility, normalization and inverse transformations are applied to map signals between dimensionless and physical domains, preserving correct amplitude and time scales across the hybrid interface.

Analog-Discrete Synchronization

The block diagram for investigating the possibility of analog-discrete synchronization is outlined in Fig. 3.4. The y_1 state variable of the hardware-based drive oscillator substitutes y_2 of the MATLAB-based response discrete-time oscillator. As a result, x_2 should repeat the behavior of x_1, and z_2 should repeat the behavior of z_1, evaluated using Pearson correlation.

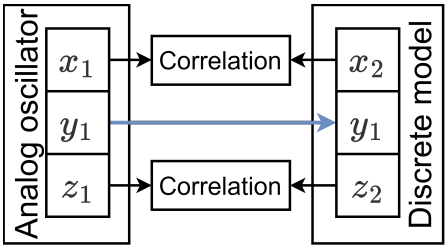


Fig. 3.4. Analog-discrete Pecora–Carroll synchronization using the hardware and discrete model.

The results of computing the 10^6 sample Pearson correlation for the analog-discrete synchronization are shown in Table 3.3. The results compiled in Table 3.3 confirm that the analog-discrete chaotic synchronization was achieved, indicated by the Pearson correlation coefficient values exceeding 0.9 for all considered state variables of the chaotic oscillators.

Table 3.3
Analog-discrete synchronization evaluation using Pearson correlation coefficient

Chaotic oscillator	x_1 **and** x_2	y_1 **and** y_2	z_1 **and** z_2
Vilnius	0.99	—	0.95
RC	0.97	—	0.99
Colpitts	—	0.98	0.99

Discrete-Analog Synchronization

The block diagram for investigating the possibility of discrete-analog synchronization is outlined in Fig. 3.5. The y_2 of the hardware circuit substitutes the y_1 of the discrete model. This results in x_1 repeating the behavior of x_2 and z_1 repeating the behavior z_2. Like in the previous study, the synchronization quality is evaluated by computing the Pearson correlation for x_1 and x_2, z_1 and z_2.

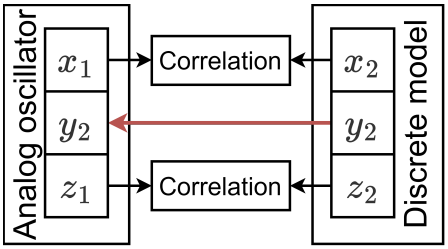


Fig. 3.5. Discrete-analog Pecora–Carroll synchronization using the hardware and discrete model.

The results of computing the 10^6 sample Pearson correlation for the discrete-analog synchronization are shown in Table 3.4. Pearson correlation coefficient in all cases equals or exceeds 0.9, thus confirming the high quality of the discrete-analog synchronization.

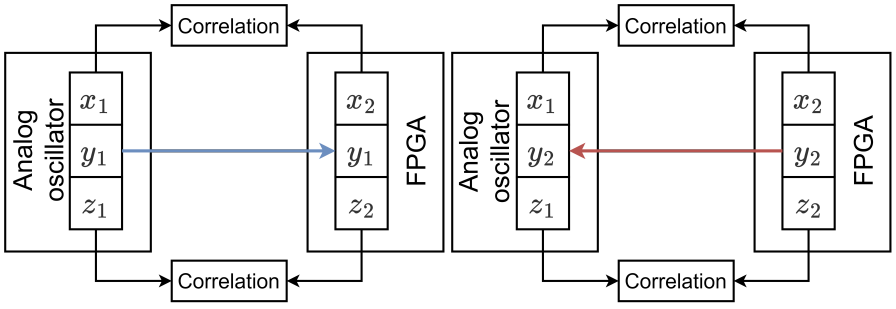
Table 3.4
Discrete-analog synchronization evaluation using Pearson correlation coefficient

Chaotic oscillator	x_1 **and** x_2	y_1 **and** y_2	z_1 **and** z_2
Vilnius	0.99	—	0.90
RC	0.99	—	0.99
Colpitts	—	0.98	0.99

3.4 Full Hardware Integration

This section verifies analog-discrete and discrete-analog synchronization between PCB-based analog oscillators and FPGA-based digital implementations, as illustrated in Fig. 3.6. In both configurations, synchronization is achieved using the Pecora–Carroll approach by substituting the corresponding state variable.

In the analog-discrete case (Fig. 3.6 (a)), the analog oscillator drives the FPGA-based oscillator, while in the reverse configuration in Fig. 3.6 (b), the roles are exchanged. In each case, the remaining state variables converge to matching behavior. Synchronization quality is evaluated using Pearson correlation.



(a) (b)

Fig. 3.6. Analog-discrete (a) and discrete-analog (b) Pecora–Carroll synchronization.

Tables 3.5 and 3.6 summarize correlation coefficients for Vilnius, RC, and Colpitts oscillators across discrete-analog and analog-discrete synchronization. Coefficients exceeding 0.9 confirm successful synchronization between analog and FPGA-based oscillators. Minor discrepancies are attributed to parameter mismatches and noise, the latter of which is analyzed in the following section.

Table 3.5
Synchronization evaluation using correlation coefficient

	Discrete-analog		**Analog-discrete**	
Chaotic oscillator	x_1 **and** x_2	z_1 **and** z_2	x_1 **and** x_2	z_1 **and** z_2
Vilnius	0.97	0.98	0.93	0.92
RC	0.72	0.97	0.89	0.90

Table 3.6
Synchronization evaluation using correlation coefficient

	Discrete-analog		**Analog-discrete**	
Chaotic oscillator	y_1 **and** y_2	z_1 **and** z_2	y_1 **and** y_2	z_1 **and** z_2
Colpitts	0.93	0.97	0.91	0.96

3.5 Discussion

This section successfully demonstrated hybrid analog-discrete and discrete-analog chaotic synchronization across multiple platforms. Key findings are as follows:

- **Robustness of the Pecora–Carroll method:** The Pecora–Carroll synchronization consistently achieved high correlation ($r > 0.9$) for Vilnius, RC, and Colpitts oscillators in both drive-response configurations.
- **Cross-domain compatibility:** Scaling transformations for voltage-to-dimensionless units and time mapping allow discrete models to accurately track physical circuits.
- **Hardware and FPGA realization:** Successful synchronization between PCB and FPGA implementations validates practical utility, despite minor discrepancies from parameter mismatches and quantization.
- **Metric validity:** The Pearson correlation coefficient proved to be a reliable measure, remaining invariant to offsets inherent in analog-to-digital conversion.

These results establish a foundation for hybrid chaotic communication systems utilizing both analog and discrete oscillators.

4 PERFORMANCE OF ANALOG-DISCRETE AND DISCRETE-ANALOG CHAOTIC SYNCHRONIZATION

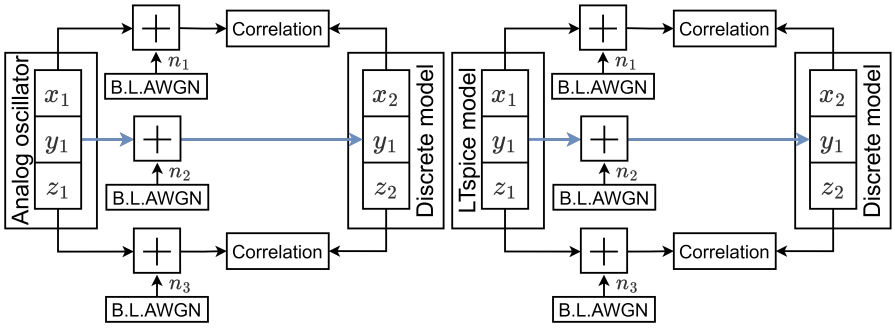
This chapter investigates the noise immunity and synchronization speed of hybrid analog-discrete and discrete-analog Pecora–Carroll synchronization. These factors are critical for evaluating robustness in real-world environments. Utilizing LTspice, MATLAB, and hardware prototypes, the study compares Vilnius and RC oscillators to assess the impact of additive noise on synchronization quality and timing. The results provide insight into the reliability, stability, and implementation trade-offs of hybrid chaotic configurations.

4.1 Synchronization Noise Immunity

This study evaluates the noise immunity of hybrid Pecora–Carroll synchronization to assess how noise impacts synchronization quality across different configurations. Utilizing LTspice, discrete models, and hardware prototypes, the analysis focuses specifically on Vilnius and RC oscillators. The following subsections detail the simulation and experimental setups and analyze the resulting performance data.

Analog-Discrete Synchronization

The first part of this study evaluates the noise immunity of analog-discrete synchronization using the experimental setup shown in Fig. 4.1. The drive system is implemented as an LTspice model or physical analog oscillator, while the response is a discrete model. Independent band-limited additive white Gaussian noise (B.L.AWGN) is added to the drive's chaotic signals, using low-pass filtering matched to the signal bandwidth. This focuses the analysis on in-band noise, which has the most significant impact on synchronization performance.



(a) (b)

Fig. 4.1. Chaotic oscillator's discrete model synchronization with LTspice model (a), and analog oscillator (b).

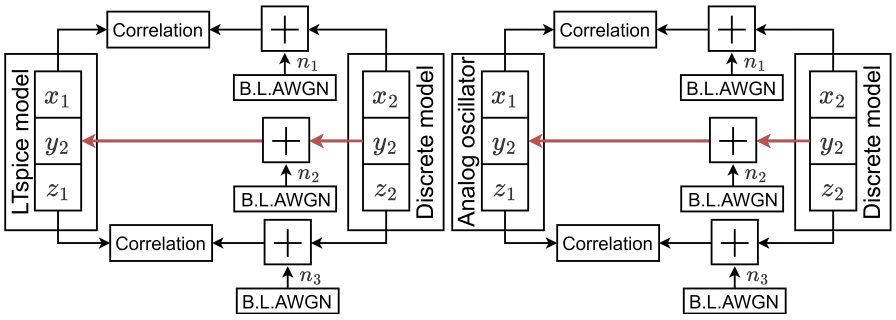
The injected noise affects the synchronization quality, leading to its degradation as the noise power increases relative to the signal power. The signal-to-noise ratio (SNR) metric is used in this study and is defined as:

$$\mathrm{SNR} = 10 \cdot \log_{10}\left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}}}\right), \tag{4.1}$$

where P_{signal} and P_{noise} are the average powers of the signals.

Discrete-Analog Synchronization

The second part of this study focuses on evaluating the noise immunity of discrete–analog synchronization. Fig. 4.2 illustrates the experimental setup. In this case, the drive chaotic oscillator is implemented as a discrete model, while the response oscillator is realized either as an LTspice model or as a physical analog oscillator. As in the first part of the study, B.L.AWGN is added to the chaotic signals of the drive oscillator.



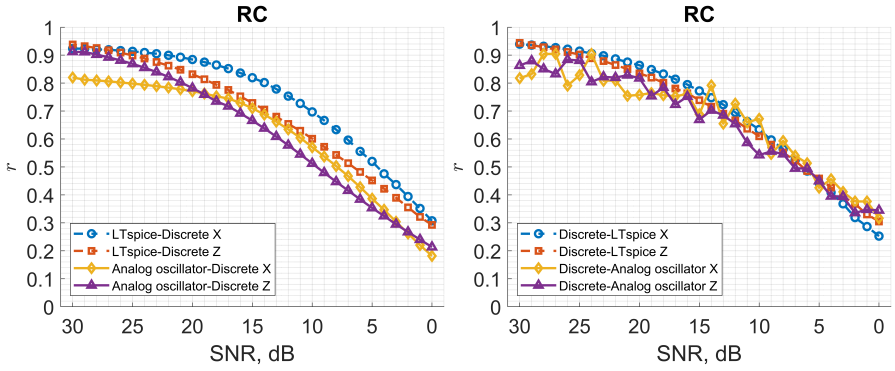
(a) (b)

Fig. 4.2. Chaotic oscillator's LTspice model (a), and hardware prototype (b) synchronization with discrete model.

Study Results

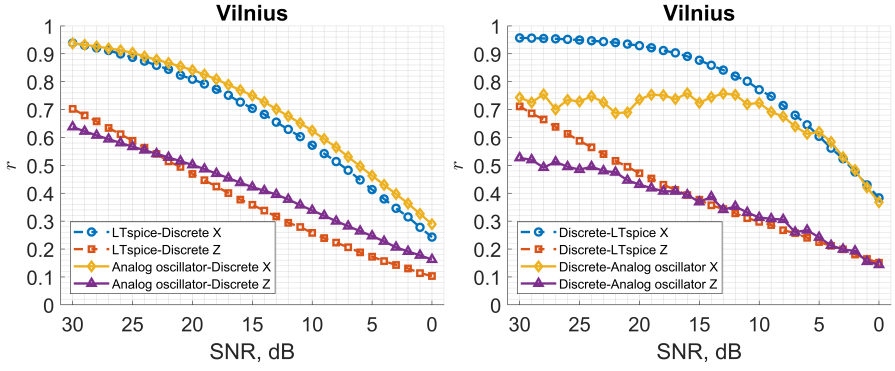
This subsection summarizes noise immunity results for analog-discrete and discrete-analog synchronization, grouped by oscillator type. As shown in Fig. 4.3 (RC) and Fig. 4.4 (Vilnius), correlation levels typically range from 0.8 to 0.95 at 30 dB SNR, dropping to 0.1–0.2 at 0 dB SNR. The exceptionally close match between LTspice and hardware results confirms that LTspice precisely predicts hardware synchronization performance, with minor discrepancies arising from hardware-specific noise and mismatches.

For the RC oscillator (Figs. 4.3 (a) and 4.3 (b)), x and z state variables perform similarly across both synchronization configurations. Conversely, Vilnius results (Figs. 4.4 (a) and 4.4 (b)) indicate the z variable is more noise-sensitive due to its waveform. Overall, the RC oscillator demonstrates superior synchronization stability across its state variables compared to the Vilnius oscillator.



(a) (b)

Fig. 4.3. Analog-discrete (a) and discrete-analog (b) synchronization noise immunity of RC chaotic oscillator.



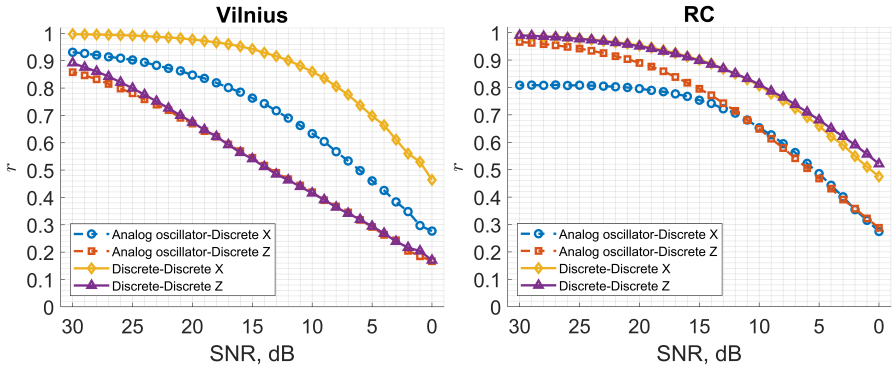
(a) (b)

Fig. 4.4. Analog-discrete (a) and discrete-analog (b) synchronization noise immunity of Vilnius chaotic oscillator.

Discrete-Discrete Synchronization Comparison

This subsection compares the noise immunity of discrete-discrete and analog-discrete synchronization for Vilnius and RC oscillators. Using the Pearson correlation coefficient r across a range of SNR, results in Fig. 4.5 shows a monotonic degradation in synchronization quality as noise increases.

The discrete-discrete configuration consistently outperforms the analog-discrete setup due to perfect parametric alignment. In contrast, analog-discrete synchronization is affected by model mismatches and physical parasitic behaviors. Despite these limitations, the analog-discrete configuration remains robust, maintaining $r > 0.5$ for SNR levels above 12 dB.



(a) (b)

Fig. 4.5. Analog-discrete and discrete-discrete synchronization noise immunity of Vilnius (a) and RC (b) chaotic oscillators.

4.2 Synchronization and De-synchronization Time

The second study on the performance of Pecora–Carroll analog-discrete and discrete-analog synchronization is synchronization and de-synchronization time. This study assesses the time required for the synchronization and de-synchronization at 30 dB SNR.

Analog-Discrete and Discrete-Analog Simulation and Experimental Setup

This study introduces a switch that controls when the synchronization signal is applied. Fig. 4.6 demonstrates the example with analog-discrete synchronization, where the synchronization signal is passed to the controlled switch before applying it to the discrete model.

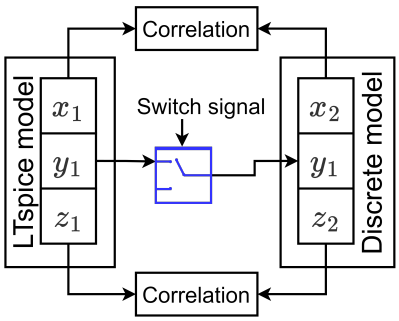


Fig. 4.6. Chaotic oscillator's discrete model synchronization with LTspice model example with the added switch to estimate synchronization and de-synchronization time.

The synchronization time is defined as the interval from the start of synchronization until the correlation reaches 80% of its maximum level. Conversely, de-synchronization time is measured from the end of the synchronization signal until correlation drops to 20% of the maximum level. All values are averaged across 10 trials.

Study Results

This subsection analyzes synchronization and de-synchronization times for the Vilnius and RC oscillators across two different configurations. Using a dimensionless time scale, Table 4.1 highlights the performance differences between analog-discrete and discrete-analog setups. The results show that analog-discrete synchronization times are generally lower, particularly for the Vilnius oscillator, suggesting that the discrete system tracks the analog drive signal more efficiently. Conversely, discrete-analog values are significantly higher, indicating that analog hardware settles more slowly when forced by signals from the discrete oscillator.

Disparities between simulation and hardware are also evident in the merged data. For the Vilnius oscillator, the hardware z de-synchronization time (1.55) is substantially lower than the LTspice prediction (8.74), suggesting that physical damping properties enhance the system's resilience. However, for the RC oscillator's x variable, the hardware synchronization time (3.29) is over triple the simulation prediction (1.04), illustrating that the physical RC circuit struggles more than idealized models to reach a stable synchronized state.

Table 4.1
Comparison of synchronization and de-synchronization times (θ) for analog-discrete and discrete-analog configurations

Oscillator	**Var.**	**Analog-discrete**				**Discrete-analog**			
		LTspice		**Hardware**		**LTspice**		**Hardware**	
		Sync	**De-sync**	**Sync**	**De-sync**	**Sync**	**De-sync**	**Sync**	**De-sync**
Vilnius	x	0.77	0.64	0.67	0.70	3.71	8.55	2.99	1.72
	z	1.00	0.50	1.00	0.33	2.37	8.74	4.85	1.55
RC	x	1.20	0.55	2.21	0.40	0.97	0.20	1.08	0.11
	z	0.97	0.20	1.08	0.11	1.04	1.52	3.29	0.76

4.3 Discussion

This section demonstrates that hybrid analog-discrete and discrete-analog synchronization schemes maintain robustness under noise, with performance degrading predictably as SNR decreases. The RC oscillator consistently outperforms the Vilnius oscillator in noise resilience across all state variables. A clear performance hierarchy emerges: discrete-discrete synchronization is the most robust due to ideal parameter matching, while analog-discrete configurations remain practical despite inherent model mismatches and analog non-idealities.

Timing analysis indicates that analog-discrete synchronization achieves faster convergence, whereas discrete-analog exhibits slower dynamics and increased sensitivity to hardware imperfections. Discrepancies between LTspice simulations and physical hardware underscore the impact of parasitics and damping. These findings offer a comprehensive evaluation of hybrid chaotic systems, providing a framework for balancing accuracy, robustness, and implementation complexity.

5 CHAOS-BASED AUTHENTICATION

Modern communication security increasingly utilizes physical-layer authentication (PLA) as a robust, hardware-based complement to traditional cryptography. By exploiting the unique dynamics of chaotic oscillators – specifically their sensitivity to parameters and noise-like appearance – PLA creates a security barrier that is difficult to replicate.

This chapter details a hardware-efficient authentication scheme using the Vilnius chaotic oscillator and a receiver capable of tracking transmitter dynamics via chaotic synchronization. We present the mathematical derivation and pipelined FPGA implementation of an adaptive least mean squares (LMS) filter designed to estimate the oscillator's internal damping parameter, a. The study concludes with an extensive performance evaluation of the estimator's digital design.

5.1 Chaotic Oscillator Parameter Estimator-Based Hardware Authentication Scheme

This section presents a chaos-based PLA scheme for wireless sensor network (WSN). Successful data transfer relies on chaotic synchronization. While chaotic carriers enhance hardware-level security, synchronization alone cannot prevent unauthorized access if a receiver connects to a similar oscillator. This necessitates a mechanism to distinguish between transmitters. Since oscillator dynamics are governed by specific parameterized equations, the proposed authentication scheme, detailed in Fig. 5.1, relies on the receiver estimating at least one internal parameter of the transmitter's chaotic oscillator.

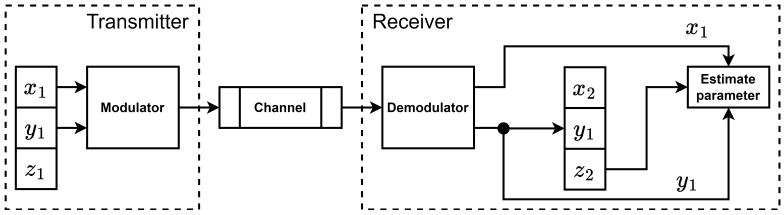


Fig. 5.1. Proposed chaos-based authentication scheme.

Fig. 5.1 illustrates the transmitter sending x_1 and y_1 signals, with y_1 used for Pecora-Carroll synchronization. The receiver utilizes received signals x_1, y_1 and the local z_2 variable to estimate a transmitter parameter. Synchronization ensures z_2 is in phase with z_1, eliminating the need to transmit all three chaotic signals.

This system supplements the existing chaos-based modulation schemes, allowing transmitter identification via a control parameter before data transfer. To prevent spoofing over public channels, this parameter must be dynamically adjusted following a pre-agreed pattern. The following sections detail the implementation and evaluation of this estimator for the Vilnius chaotic oscillator.

5.2 Vilnius Chaotic Oscillator Parameter Estimator

The first step of designing the parameter estimator is to select the parameter of the chaotic oscillator that will be estimated based on the difference equations:

$$\begin{cases} \underbrace{x[n+1]}_{\text{Next value}} = \underbrace{x[n]}_{\text{Current value}} + \underbrace{y[n]}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y[n+1]}_{\text{Next value}} = \underbrace{y[n]}_{\text{Current value}} + \underbrace{(a \cdot y[n] - x[n] - z[n])}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z[n+1]}_{\text{Next value}} = \underbrace{z[n]}_{\text{Current value}} + \underbrace{\left(\frac{b}{\varepsilon} + \frac{1}{\varepsilon} \cdot y[n] - \frac{c}{\varepsilon} \cdot (\mathrm{e}^{z[n]} - 1)\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{5.1}$$

By observing the system (5.1), the most convenient parameter for estimation is a from the second term of the difference equations expressed as:

$$a_{estimated}[n] = \frac{\frac{y[n+1]-y[n]}{\Delta\theta} + x[n] + z[n]}{y[n]}. \tag{5.2}$$

The convenience is that the equation contains only one parameter and that the signal relations are linear, unlike other terms of the system (5.1).

Digital Implementation of the Parameter Estimator

The digital design of the a parameter estimator is divided into two components: first, the numerator is acquired from (5.2):

$$s[n] = \frac{y[n+1] - y[n]}{\Delta\theta} + x[n] + z[n], \tag{5.3}$$

second, the estimated value of a is acquired from the expression:

$$a_{estimated}[n] = \frac{s[n]}{y[n]}. \tag{5.4}$$

The digital implementation of the first component, shown in Fig. 5.2, uses a fixed-point arithmetic pipeline. The value $s[n]$ is computed from $x[n]$, $z[n]$, and $\frac{y[n]}{\Delta\theta}$ as per (5.3). Since the time step is a power of two, $\frac{y[n]}{\Delta\theta}$ is efficiently calculated using bit shifting. This process involves four registers, introducing a four-clock-cycle delay. To ensure $s[n]$ and $y[n]$ remain in phase for the calculation in (5.4), a digital delay line is used to produce the synchronized signal $y_{delayed}[n]$.

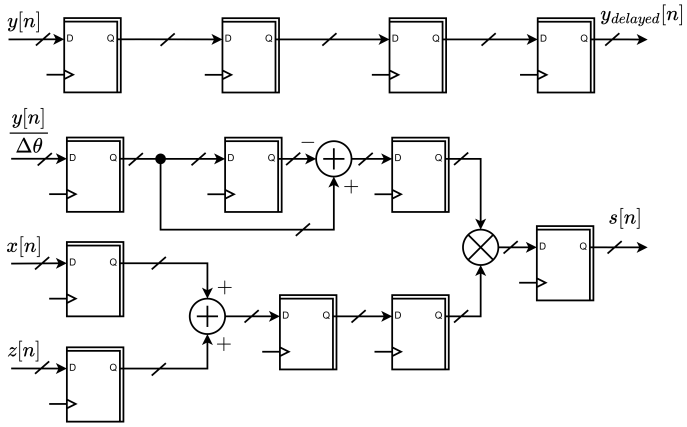


Fig. 5.2. Pipeline design for acquiring the numerator par of the a parameter estimator.

The second component's digital implementation is more complex, as signal division cannot be performed in a single clock cycle. Instead, an adaptive LMS filter (Wiener filter with minimum mean squared error (MMSE)) is employed to obtain $a_{estimated}[n]$. Using $y_{delayed}[n]$, the relationship in (5.4) is expressed as

$$a_{estimated}[n] \cdot y_{delayed}[n] = s[n]. \tag{5.5}$$

Then, $a_{estimated}[n]$ can be assessed using the stochastic gradient as

$$a_{estimated}[n+1] = a_{estimated}[n] + 2\mu \cdot y_{delayed}[n] \cdot \left(s[n] - a_{estimated}[n] \cdot y_{delayed}[n]\right). \tag{5.6}$$

The constant μ represents the step size or convergence speed, determining how quickly the algorithm reaches the Wiener MMSE solution. It must be carefully selected: a μ value that is too low causes slow convergence, while an excessively high value induces output oscillations.

Fig. 5.3 illustrates the digital implementation of the LMS adaptive filter based on (5.6). The filter utilizes a pipelined feedback structure, receiving $s[n]$ and $y_{delayed}[n]$ from the numerator pipeline. To optimize the fixed-point arithmetic, the convergence constant 2μ is set to 1×10^{-5} and floored to the nearest power of two, enabling multiplication via bit-shifting. Due to the small step size, $a_{estimated}[n]$ is represented with 4 integer and 20 fractional bits.

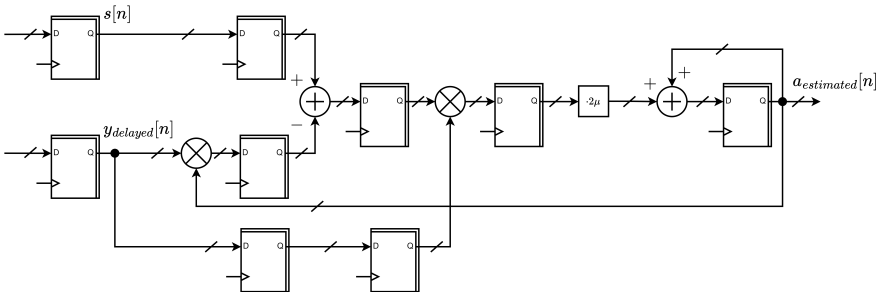
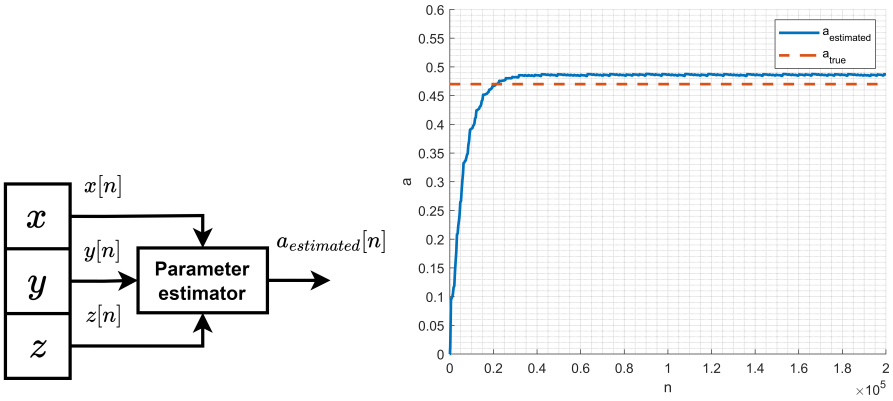


Fig. 5.3. The digital implementation of the LMS adaptive filter for parameter a estimation.

Performance Evaluation

This subsection evaluates the performance of the designed parameter estimator for the Vilnius chaotic oscillator. The initial test, illustrated in Fig. 5.4, utilizes the block diagram shown in Fig. 5.4 (a), where discrete signals $x[n]$, $y[n]$, and $z[n]$ are passed to the estimator with parameter a fixed at 0.47.

As shown in Fig. 5.4 (b), $a_{estimated}[n]$ rapidly converges from zero to a stable value of 0.485 within 4×10^4 clock cycles, exhibiting minimal ripple. While this output stays close to the true value (indicated by the dashed line), the slight discrepancy exists because the LMS algorithm converges to the best linear MMSE estimator of $s[n]$ from $y_{delayed}[n]$ rather than the exact physical parameter.



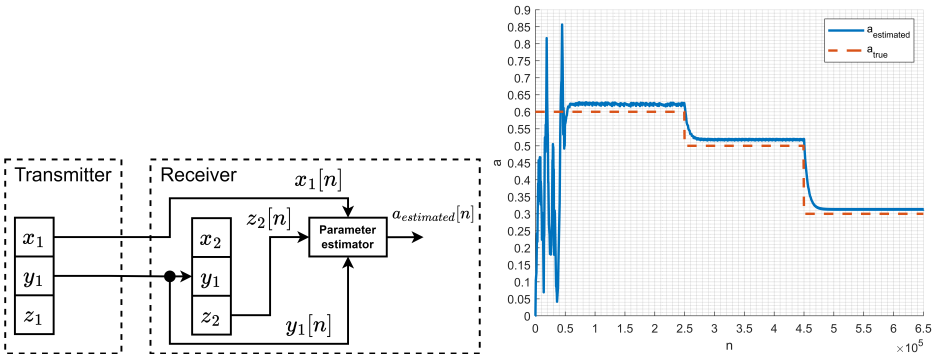
(a) (b)

Fig. 5.4. Experimental setup for verifying the a parameter estimator (a) and the output of the a parameter estimator (b).

The second test evaluates the estimator's ability to track the transmitter's parameter a while the receiver is synchronized via the Pecora–Carroll approach. As shown in the verification setup (Fig. 5.5 (a)), the transmitter sends $x_1[n]$ and $y_1[n]$ to the receiver; synchronization is initiated after 5×10^4 clock cycles.The receiver uses the received $x_1[n]$, $y_1[n]$, and its local $z_2[n]$ variable to estimate the transmitter's parameter. This configuration directly implements the authentication scheme

proposed in Fig. 5.1. While the receiver's internal a remains fixed at 0.47, the transmitter's parameter is stepped through values of 0.6, 0.5, and 0.3 every 2×10^5 clock cycles post-synchronization.

Fig. 5.5 (b) displays the $a_{estimated}[n]$ output. During the initial 5×10^4 clock cycles, the oscillators are asynchronous, and $a_{estimated}[n]$ remains unstable as expected. Once synchronized, the estimator successfully tracks the transmitter's parameter a, reaching stable levels of 0.61, 0.51, and 0.31, respectively. Similar to previous results, the signal exhibits minor ripples and a transition time of approximately 4×10^4 cycles.

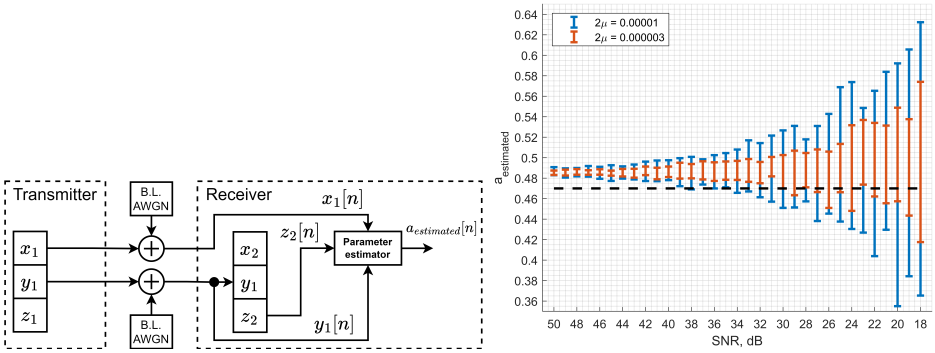


(a) (b)

Fig. 5.5. Experimental setup for verifying the a parameter estimator in synchronous mode (a) and the output of the a parameter estimator (b).

The next study investigates the impact of additive noise on estimator performance. As shown in Fig. 5.6 (a), B.L.AWGN is added to the transmitter's $x_1[n]$ and $y_1[n]$ signals. This noise is in-band, representing a worst-case scenario where simple filtering cannot improve the SNR. Because the system relies on synchronous operation, this noise simultaneously degrades both synchronization and parameter estimation. For this test, receiver's and transmitter's a parameters are fixed at 0.47, while the SNR is varied from 18 dB to 50 dB.

The results, presented in Fig. 5.6 (b), first examine the original convergence speed ($2\mu = 1 \times 10^{-5}$). As SNR decreases, the min-max range of $a_{estimated}$ expands significantly, which may hinder the ability to distinguish between authentication levels. To improve noise resilience, a second test was conducted with a reduced convergence speed ($2\mu = 3 \times 10^{-6}$). By increasing the adaptive filter's effective window, this adjustment noticeably narrows the min-max range for the same SNR levels, enhancing stability at the cost of convergence time.



(a) (b)

Fig. 5.6. Experimental setup for verifying the *a* parameter estimator in B.L.AWGN channel (a) and the output of the *a* parameter estimator (b).

5.3 Discussion

This section introduced a novel PLA scheme based on chaotic oscillator parameter estimation. Integrating this mechanism into chaos-based data transfer systems provides a robust authentication layer by allowing the receiver to verify specific transmitter parameters.

Performance evaluation identified several critical factors for deployment.

- **Time vs. precision tradeoff:** Estimation time is governed by the convergence speed. While faster convergence reduces latency, it increases output fluctuations, potentially hindering the ability to distinguish between discrete parameter ranges.
- **Noise immunity:** Since fluctuations increase with noise, convergence speed must be adjusted according to the channel state. In this system, the channel state can be monitored using the Pearson correlation coefficient – already used for data detection – to evaluate synchronization quality and guide estimator adjustments.
- **System configurability:** The receiver's native oscillator parameter dictates which transmitter values are most distinguishable. This allows for a highly configurable architecture where users can set native parameters and adapt convergence speeds to define precise authentication ranges.

Combined, these features create a highly parameterized system that effectively mitigates unauthorized data transmission from similar architectures.

CONCLUSIONS

This Doctoral Thesis has presented a comprehensive study on the analysis, design, and experimental validation of analog-discrete chaotic systems and their synchronization.

The results demonstrate that chaotic synchronization between analog circuits and FPGA-based digital models is both feasible and reliable. High levels of synchronization accuracy were achieved, confirming that discrete-time implementations can effectively reproduce the dynamics of continuous-time chaotic systems and vice versa when appropriate scaling and normalization techniques are applied.

The research further shows that FPGA-based implementations using fixed-point arithmetic are capable of preserving essential chaotic properties, making them suitable for real-time and hardware-efficient applications. Among the investigated configurations, analog-discrete synchronization exhibited the highest robustness, while discrete-analog configuration also provided satisfactory performance under practical conditions. Although noise, quantization effects, and component tolerances introduce deviations from ideal behavior, the systems maintained stable synchronization within acceptable limits, demonstrating their robustness in real-world environments.

In addition, the feasibility of chaos-based authentication was validated through parameter estimation techniques. The results indicate that chaotic systems can be effectively utilized for physical-layer security applications, offering a promising alternative to conventional methods.

In summary, this Thesis establishes a unified framework for the development and implementation of analog-discrete chaotic systems, contributing to the advancement of secure communication technologies and hardware-based security solutions.

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